# Lab 2 Behavioral Report

Academic Integrity (more info @ https://aisc.uci.edu/): You are encouraged to discuss the labs at a high level, but the code/equations/simulations you come up with should be your own. By typing “yes” at the end of this question and filling in your name, you certify that the work you are turning in is your own work. Is the work you are turning in your own? \_\_\_

If you worked on any portion of your report or vhdl code with other students (discussion at high level & debugging; if more, please describe), please list their names here: Wonhee Lee

Student Name: Wonhee Lee  
Student ID: 54872959  
Date Completed: 2020-04-25  
Time Spent: Reviewing Digital Design Material: 30 min  
 Design/Preparation Work: 1 h 30 min  
 VHDL Coding & Debugging: 3 h

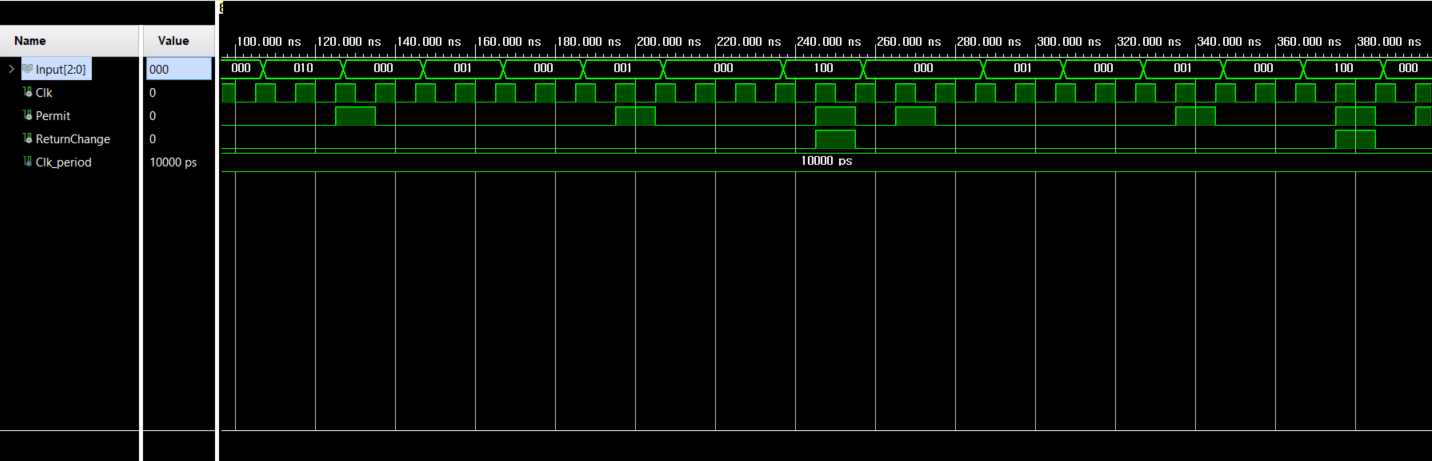
## Behavioral Overview

80%  
Done with basic logics for the project, but still have to fix the problem with the clock and the output.

## Lab 2 FSM



## Lab 2 Behavioral Simulation Graph



Seems like the clock cycle is too short that makes the machine to think that there were input twice, although there was only one. That is why there are points where Permit goes to 1 even though it should not.